CLAIMS

1. A layered wiring device comprising a plurality of electrical conduction members defining at least one electrical conduction path though a layered substrate, the at least one electrical conduction path having substantial impedance continuity maintained within a predefined limit therealong.

2. A layered wiring device as claimed in claim 1, the layered substrate including a dielectric core member, the substantial impedance continuity accomplished at least in part by at least one of: only one electrical conduction path lamination layer on opposing sides of the dielectric core member; a different number of electrical conduction path lamination layers on opposite sides of the dielectric core member; a different dielectric separation distance between electrical conduction path lamination layers on either side of the dielectric core member in comparison to other dielectric separation distances of electrical conduction path lamination layers of the layered substrate; and a different dielectric permittivity of a material of the dielectric core member in comparison to a permittivity of a material of dielectric lamination layers of the layered substrate.

3. A layered wiring device as claimed in claim 1, the layered substrate being a laminated substrate having a dielectric core member and at least one dielectric lamination layer, the dielectric core member having one of: a thickness which is thicker than a thickness of the at least one dielectric lamination layer, and material of a different dielectric permittivity that that of a material of the at least one dielectric lamination layer, at least one electrical conduction member of the at least one electrical conduction path being disposed on a first side of the dielectric core member, while other ones of the plurality of electrical conduction members having a potential parasitic capacitance relationship with

the at least one electrical conduction member being disposed on an opposite side of the dielectric core member.

4. A layered wiring device as claimed in claim 3, with only one electrical conduction lamination layer being disposed on the first side of the dielectric core member, and with the at least one electrical conduction member being a portion of the one electrical conduction lamination layer.

5. A layered wiring device as claimed in claim 4, the at least one electrical conduction member including at least one of a conductive bump/ball, trace, pad and via-pad member of a grid array mounting arrangement.

6. A layered wiring device as claimed in claim 5, where the layered wiring device is part of the laminated substrate of a semiconductor package.

7. A layered wiring device as claimed in claim 3, the layered wiring device being part of NGIO hardware.

8. A system comprising: a layered wiring device including a plurality of electrical conduction members defining at least one electrical conduction path though a layered substrate, the at least one electrical conduction path having substantial impedance continuity maintained within a predefined limit therealong.

9. A system as claimed in claim 8, the layered substrate including a dielectric core member, the substantial impedance continuity accomplished at least in part by at least one of: only one electrical conduction path lamination layer on opposing sides of the dielectric core member; a different number of electrical conduction path lamination layers on opposite sides of the dielectric core member; a different dielectric separation distance between electrical conduction path lamination layers on either side of the dielectric core member in comparison to other dielectric separation distances of electrical conduction path lamination layers of the layered substrate; and, a different dielectric permittivity of a material of the dielectric core member in comparison to a permittivity of a material of dielectric lamination layers of the layered substrate.

10. A system as claimed in claim 8, the layered substrate being a laminated substrate having a dielectric core member and at least one dielectric lamination layer, the dielectric core member having one of: a thickness which is thicker than a thickness of the at least one dielectric lamination layer, and material of a different dielectric permittivity that that of a material of the at least one dielectric lamination layer, at least one electrical conduction member of the at least one electrical conduction path being disposed on a first side of the dielectric core member, while other ones of the plurality of electrical conduction members having a potential parasitic capacitance relationship with the at least one electrical conduction member being disposed on an opposite side of the dielectric core member.

11. A system as claimed in claim 10, with only one electrical conduction lamination layer being disposed on the first side of the dielectric core member, and with the at least one electrical conduction member being a portion of the one electrical conduction lamination layer.

12. A system as claimed in claim 11, the at least one electrical conduction member including at least one of a conductive bump/ball, trace, pad and via-pad member of a grid array mounting arrangement.

13. A system as claimed in claim 12, where the layered wiring device is part of the laminated substrate of a semiconductor package.

14. A system as claimed in claim 10, the layered wiring device being part of NGIO hardware.

15. A layered wiring device comprising lamination means including a plurality of electrical conduction members defining at least one electrical conduction path though a layered substrate, for providing substantial impedance continuity maintained within a predefined limit along the at least one electrical conduction path.

16. A layered wiring device as claimed in claim 15, the lamination means comprising a dielectric core member, the substantial impedance continuity accomplished at least in part by at least one of: only one electrical conduction path lamination layer on opposing sides of the dielectric core member; a different number of electrical conduction path lamination layers on opposite sides of the

dielectric core member; a different dielectric separation distance between electrical conduction path lamination layers on either side of the dielectric core member in comparison to other dielectric separation distances of electrical conduction path lamination layers of the layered substrate; and, a different dielectric permittivity of a material of the dielectric core member in comparison to a permittivity of a material of dielectric lamination layers of the layered substrate.

17. A layered wiring device as claimed in claim 15, the lamination means comprising a laminated substrate having a dielectric core member and at least one dielectric lamination layer, the dielectric core member having one of: a thickness which is thicker than a thickness of the at least one dielectric lamination layer, and material of a different dielectric permittivity that that of a material of the at least one dielectric lamination layer, at least one electrical conduction member of the at least one electrical conduction path being disposed on a first side of the dielectric core member, while other ones of the plurality of electrical conduction members having a potential parasitic capacitance relationship with the at least one electrical conduction member being disposed on an opposite side of the dielectric core member.

18. A layered wiring device as claimed in claim 17, with only one electrical conduction lamination layer being disposed on the first side of the dielectric core member, and with the at least one electrical conduction member being a portion of the one electrical conduction lamination layer.

19. A layered wiring device as claimed in claim 18, the at least one electrical conduction member including at least one of a conductive bump/ball, trace, pad and via-pad member of a grid array mounting arrangement.

20. A layered wiring device as claimed in claim 19, where the lamination means is part of the laminated substrate of a semiconductor package.

21. A layered wiring device as claimed in claim 17, the layered wiring device being part of NGIO hardware.